In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	Ex Parte Reexamination of 6,426,916
				Filing Date	Herewith
				Applicant(s)	...
				Art Unit	*To be Determined*
				Examiner Name	*To be Determined*
SHEET	1 (Exhibits)	OF	3 (Exhibits)	Attorney Docket Number	38512.3

U. S. PATENT DOCUMENTS

Examiner's Initials	Exhibit	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
	A	6,426,916	07-30-2002	Farmwald, et al.
	B	5,590,086	12-31-1996	Park, et al.
	F	4,480,307	10-30-1984	Budde, et al.
	G	4,315,308	02-09-1982	Jackson
	J	4,933,910	06-12-1990	Olson, et al.
	K	5,361,277	03-30-1989	11-01-1994

FOREIGN PATENT DOCUMENTS

Examiner's Initials	Exhibit	Foreign Patent Document	Publication Date MM-DD-YYYY	Patentee or Applicant of Cited Document	Translation Y/N
	I	JP S56-047996	04-30-1981	Yoshida	Yes
	L	GB 2187553	05-18-1988	Lofgren, et al.	

NON-PATENT LITERATURE DOCUMENTS

Examiner's Initials	Exhibit	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	C	Joint Electron Device Engineering Council (JEDEC) Standard No. 21-C, Revision 9 published in 1999 ("JEDEC Standard")
	D, Tab 1	Hyundai, HY5DV651622, Rev. 0.9, published January 2000 ("Hynix -1")
	D, Tab 2	Hyundai, SDRAM Timing Diagram, Rev. 1.2, published December 1999 ("Hynix -2")
	D, Tab 3	Hyundai, DDR SDRAM DEVICE OPERATION, Rev. 0.2, published December 1998 ("Hynix -3")
	E, Tab 1	Intel Corporation, IAPX 432 Interconnect Architecture Reference Manual, published in 1982 ("the IAPX Manual")
	E, Tab 2	Intel Corporation, Electrical Specifications for IAPX 43204 Bus-Interface Unit (BIU) and IAPX 43205 memory control unit (MCU), published March 1983 ("the IAPX Specification")
	H	Rau et al., The Cydra 5 Departmental Supercomputer Design Philosophies, Decisions, and Trade-offs, published in January 1989 ("Rau")

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

Customer No. 000027683

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			Complete if Known	
				Application Number	Ex Parte Reexamination of 5,794,060
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Filing Date	Herewith
				Applicant(s)	...
				Art Unit	*To be Determined*
				Examiner Name	*To be Determined*
SHEET	2 (Exhibits)	OF	3 (Exhibits)	Attorney Docket Number	33142.9

NON-PATENT LITERATURE DOCUMENTS		
Examiner's Initials	Exhibit	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	M	Johnson et al., A Variable Delay Line PLL for CPU – Coprocessor Synchronization, IEEE Journal of Solid-State Circuits, vol. 23, no. 5, published October 1988 ("Johnson")
	N	Intel Corporation, Memory Components Handbook, Chapter 1 and Chapter 3, Application Note AP-132, published in 1982 and 1985 ("the iRAM reference")
	O	Claim chart for claims 1-5, 10, 12-16, 18-20, 23, 25-32, 35, 37, and 39-41 based on Park, with additional reference to the JEDEC Standard
	P	Claim chart for claims 1-5, 9-10, 12-16, 18-20, 23, 25-27, 30-32, 35, 37, and 40-41 based on the JEDEC Standard
	Q	Claim chart for claims 1-41 of the '916 patent based on the iAPX Manual, with additional reference to Rau, Yoshida, Olson, Johnson, Lofgren, and Grover
	R	Claim chart for claims 1-41 of the '916 patent based on Budde, with additional reference to Rau, Yoshida, Olson, Johnson, Lofgren, and Grover
	S	Patent Family Tree Chart
	T	File History of the '916 patent
	U	File History of U.S. Patent No. 6,452,863 ("the '863 parent patent") (Tab 1 identifies the original disclosure of the '863 parent patent, and Tab 2 identifies the remaining portions of the file history)
	V	*Rambus Inc. v. Samsung Electronics Ltd., et al.* No. C 05 02298 RMW (N.D. Cal. 2006), Preliminary Infringement Contentions
	W	*Samsung Electronics Co., Ltd., v. Rambus Inc.* No. 3:05cv406 (E.D. Va. 2006), Memorandum Opinion filed July 18, 2006
	X	*Hynix Semiconductor, Inc. et al. v. Rambus Inc.*, No. CV 00-20905 RMW (N.D. Cal. 2005), Joint Claim Construction and Prehearing Statement Pursuant to Patent Local Rule 4-3
	Y	*Hynix Semiconductor, Inc. et al. v. Rambus Inc.*, No. CV 00-20905 RMW (N.D. Cal. 2005), Claim Construction Order filed Nov. 15, 2004
	Z	Selected Excerpts from the Trial Transcript from *Hynix Semiconductor, Inc. et al. v. Rambus Inc.*, No. CV 00-20905 RMW (N.D. Cal. 2005).
	AA	*Rambus Inc. v. Infineon Technologies et al.*, No. 3:00cv524 (E.D. Vir. 2001), Memorandum Opinion
	AB	*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081 (Fed. Cir. 2003)

Examiner Signature		Date Considered	

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				Filing Date	Herewith
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				Art Unit	*To be Determined*
				Examiner Name	*To be Determined*
SHEET	3 (Exhibits)	OF	3 (Exhibits)	Attorney Docket Number	33142.9

NON-PATENT LITERATURE DOCUMENTS

Examiner's Initials	Exhibit	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	AC	Waters, Hynix Told To Pay Damages To Rambus, Financial Times, April 24 2006
	AD	Poletti, Rambus wins victory from Supreme Court - Win Could Lead To Success For Rambus' Other Lawsuits Seeking Royalties, San Jose Mercury News, Oct. 07, 2003
	AE	Kanellos, Future of memory market hangs on Rambus trials - It's the trial of the century, at least as far as the memory industry is concerned, CNET News.com, Feb. 12, 2001, http://news.com.com/Future+of+memory+market+hangs+on +Rambus+trials/2100-1001_3-252404.html
	AF	Appeal Board Decision dated Feb. 12, 2004, Summary of Facts and Submissions for the oppositions filed against European Patent No. 0 525 068
	AG	Summary of Facts and Submissions for the oppositions filed against European Patent No. 1 004 956
	AH, Tab 1	In the Matter of Rambus, Inc., FTC Docket No. 9302, Opinion of the Commission
	AH, Tab 2	In the Matter of Rambus, Inc., FTC Docket No. 9302, Concurring Opinion of Commissioner Jon Leibowitz
	AH, Tab 3	In the Matter of Rambus, Inc., FTC Opinion Docket No. 9302, Order Reversing and Vacating Initial Decision ...
	AI, Tab 1	Rambus' Final Infringement Contentions in the Hynix Litigation
	AI, Tab 2	Exhibit A (accused products) to Rambus' Final Infringement Contentions
	AI, Tab 3	Exhibit P ('916 infringement chart) to Rambus' Final Infringement Contentions
	AI, Tab 4	Exhibit R (Exemplary data sheet) to Rambus' Final Infringement Contentions
	AJ	CD-ROM including present Request for *Inter Partes* Reexamination and Exhibits

Examiner Signature		Date Considered	

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